Optimum Design of Asymmetrical Multisection Two-Way Power Dividers With Arbitrary Power Division and Impedance Matching

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***Abstract*—A general analysis and design procedure is developed for the asymmetrical multisection power divider with arbitrary power division ratio and arbitrary specifications of input and output impedance matching over any desired frequency bandwidth. The even- and odd-mode analysis, which was previously applied to the design of multisection Gysel power dividers, required that the unequal power division ratios be accompanied with appropriately proportional output impedances. This requirement is relaxed here. The equivalent circuits are first obtained for the divider and then their scattering parameters are determined. Some error functions are then constructed by the method of least squares. Their minimization determines the geometrical dimensions of the optimum divider. An approximate method based on the even and odd modes is developed for its initial design of the divider. Two examples of single- and double-section dividers are designed. Their frequency responses of isolation and transmission coefficients are obtained by the proposed method, HFSS software, fabrication, and measurement. They agree within the approximate assumptions. A two-section and two-way power divider is designed and fabricated by the proposed method for the case of unequal port impedances in the L-band. The measured isolation between the outputs is better than −22 dB in 44% of the band.**

***Index Terms*—Gysel power divider, impedance matching, method of least squares, power dividers, Wilkinson power divider.**

I. Introduction

POWER dividers and combiners are widely used in various microwave devices and systems, such as microwave power amplifiers, linearization of power amplifiers, test setups, and measurement circuits. Power dividers with unequal power division and impedance matching among the input and output ports also find applications in antenna arrays for the synthesis and shaping of radiation patterns. The isolation among outputs is a crucial design consideration of power dividers and directional couplers. High wideband isolation reduces the spurious coupling among active components and actually decreases the out-of-band oscillations and positive feedback in the networks. The Gysel power divider has been proposed for microstrip structures for power transmission with the provision of heat transfer to the ground plane through some resistors. Its power-handling capability is up to 10 and 5 kW in the L- and S-bands, respectively, which is obviously dependent on the thermal resistance of resistors and the heat sinks. It is ultimately limited to the thermal capacity and dielectric strength of the transmission lines [1]. However, its narrow frequency bandwidth limits its applications. The design optimization of the Gysel N-way power divider is given in [2]. However, the power is equally divided among the outputs and its isolation bandwidth is also narrow.

A design procedure is given in [3] for the multisection Gysel power divider based on the even- and odd-mode analysis with the objective of increasing the isolation bandwidth. However, this method may be applied only for the case of equal power division among the output ports. The impedances at ports 2 and 3 should also be equal. The even- and odd-mode analysis was extended in [4] for the design of Wilkinson power dividers with unequal output power division ratios. A procedure for the design of Gysel power dividers with unequal power division ratios at the output is provided in [5]. On the other hand, the applications of these methods bring about several limitations. That is, the characteristic impedances of corresponding transmission lines (on the upper and lower sections of divider) should be proportional to each other by the ratio of specified power division, in order that the two halves of the circuit are electrically symmetric. Consequently, it is necessary that the impedance values at the output ports be proportional to the specified power division ratio. This raises the requirement for additional impedance-matching circuits at the output ports, which eventually leads to the increase of circuit size. Furthermore, since the frequency dispersion and power loss properties of microstrip transmission lines depend on their characteristic impedances, for the case of unequal power division, it is not feasible to adjust line impedances to make the device electrically symmetric. Furthermore, single section configurations have been used, which have narrow bandwidths of isolation among the outputs and transmission coefficients.

A design procedure for power dividers with arbitrary power division ratios and impedance matching among the terminal ports for asymmetrical passive networks is available in the literature [6], [7]. A general method (without resorting to the even- and odd-mode analysis) has been presented in [8] for the optimum design of the Wilkinson power divider for arbitrary power division and impedance matching. However, these methods have not been applied to high power dividers to date.

In this paper, we propose to extend such a method for the optimum design of a high power divider to realize the same features. In Section II, we use the proposed method to determine the scattering parameters in the general case of a power divider. In Section III, we present a method for the initial design of its geometrical structure and also its final optimum de-

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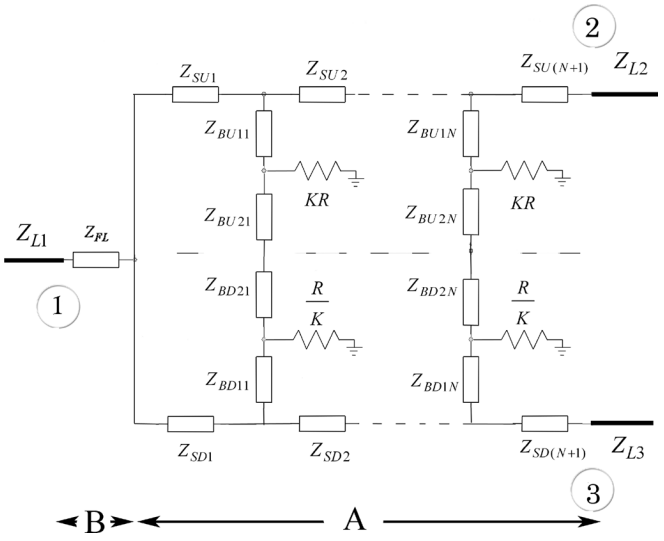


Fig. 1. Sructure of a general power divider.

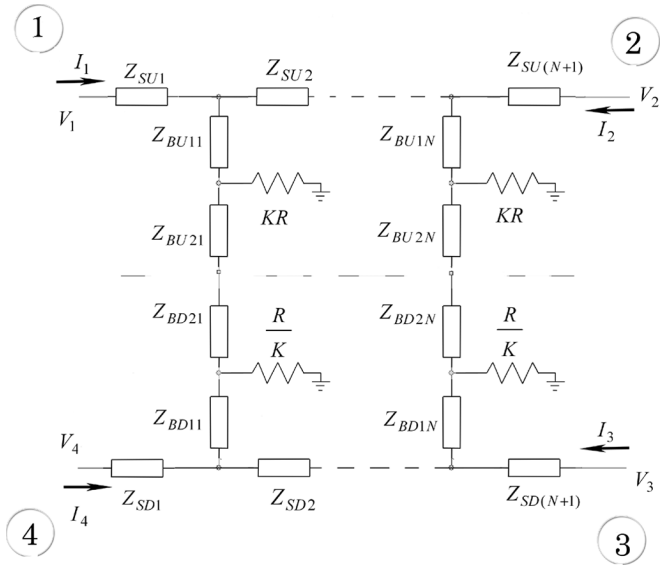


Fig. 2. Transformation of three-port network A in Fig. 1 to a four-port network.

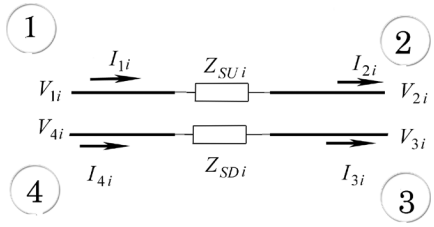


Fig. 3. Two corresponding transmission lines.

sign. In Section IV, several examples of the design procedure are presented and results are compared with full-wave simulation software, such as Ansoft HFSS, version 11 [9]. Two prototype models are fabricated and tested, which verify the proposed method of optimum design of the general power divider.

II. Computation of Scattering Parameters

The schematic diagram of a two-way N-section power divider with arbitrary impedances at its input and output ports and arbitrary power division at its outputs, which is in the ratio of K^2 (at port 3) to 1(at port 2), is drawn in Fig. 1.

The divider is composed of N-sections in order to increase its effective bandwidth. In the case that the line section impedances in the upper half circuit are not proportional to those in the lower one, the voltage distributions on them will not be equal to each other. Accordingly, the circuit configuration in Fig. 1 is divided into two sections:A and B.

We then cut the input of A into two inputs, called 1 and 4 for the purpose of subsequent analysis, as shown in Fig. 2.

This network may be decomposed into two subsections,which are: 1) the series line sections in the main upper and lower half circuits, as shown in Fig. 3, and 2) the branch line sections between the upper and lower halves, as shown in Fig. 4.

We first obtain the $ABCD$ matrix of the ith section in the upper transmission line at mth frequency as in Fig. 3

$$\begin{bmatrix} V_{1i} \\ I_{1i} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_{2i} \\ I_{2i} \end{bmatrix} = \begin{bmatrix} \cosh(\gamma_{i,m} l_i) & Z_{0,i,m} \sinh(\gamma_{i,m} l_i) \\ Y_{0,i,m} \sinh(\gamma_{i,m} l_i) & \cosh(\gamma_{i,m} l_i) \end{bmatrix} \begin{bmatrix} V_{2i} \\ I_{2i} \end{bmatrix}. \tag{1}$$

The $ABCD$ matrix of the whole four-port network of the ith section in Fig. 3 will then be presented by (2), shown at the bottom of the page.

$$\begin{bmatrix} V_{1i} \\ V_{4i} \\ I_{1i} \\ I_{4i} \end{bmatrix} = \begin{bmatrix} \cosh(\gamma_{SUi,m} l_{SUi}) & 0 & Z_{SU,i,m} \sinh(\gamma_{SUi,m} l_{SUi}) & 0 \\ 0 & \cosh(\gamma_{SDi,m} l_{SDi}) & 0 & Z_{SD,i,m} \sinh(\gamma_{SDi,m} l_{SDi}) \\ Y_{SU,i,m} \sinh(\gamma_{SUi,m} l_{SUi}) & 0 & \cosh(\gamma_{SUi,m} l_{SUi}) & 0 \\ 0 & Y_{SD,i,m} \sinh(\gamma_{SDi,m} l_{SDi}) & 0 & \cosh(\gamma_{SDi,m} l_{SDi}) \end{bmatrix} \times \begin{bmatrix} V_{2i} \\ V_{3i} \\ I_{2i} \\ I_{3i} \end{bmatrix} = [P]_{i,m} \begin{bmatrix} V_{2i} \\ V_{3i} \\ I_{2i} \\ I_{3i} \end{bmatrix} \tag{2}$$

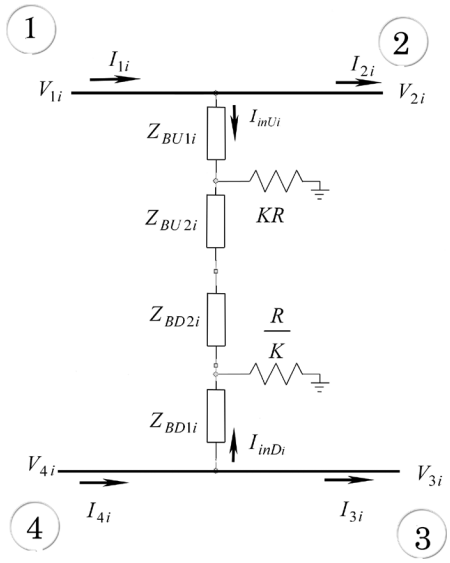


Fig. 4. ith branch line.

Next, we obtain the $ABCD$ matrix of the ith branch line in Fig. 4. The currents at the nodes among the series lines and parallel branches are now related as

$$\begin{aligned} I_{1i} &= I_{2i} + I_{inUi} \\ I_{4i} &= I_{3i} + I_{inDi}. \end{aligned} \tag{3}$$

The admittance matrix representation of the ith branch is

$$\begin{aligned} \begin{bmatrix} I_{inUi} \\ I_{inDi} \end{bmatrix} &= \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_{2i} \\ V_{3i} \end{bmatrix} \\ &= \begin{bmatrix} \dfrac{D}{B} & \dfrac{BC-AD}{B} \\ -\dfrac{1}{B} & \dfrac{A}{B} \end{bmatrix} \begin{bmatrix} V_{2i} \\ V_{3i} \end{bmatrix}. \end{aligned} \tag{4}$$

The overall $ABCD$ matrix parameters of the ith branch of the divider equivalent circuit [as denoted in (4)] are

$$\begin{aligned} \begin{bmatrix} A & B \\ C & D \end{bmatrix} &= T_{BU1i,m} \times T_{KR} \times T_{BU2i,m} \times T_{BD2i,m} \\ &\quad \times T_{R/K} \times T_{BD1i,m} \end{aligned} \tag{5}$$

where the $ABCD$ matrices of the transmission lines and those of the resistors are

$$\begin{aligned} T_{Bx} &= \begin{bmatrix} \cosh(\gamma_{Bx} l_{Bx}) & Z_{0Bx} \sinh(\gamma_{Bx} l_{Bx}) \\ Y_{0Bx} \sinh(\gamma_{Bx} l_{Bx}) & \cosh(\gamma_{Bx} l_{Bx}) \end{bmatrix} \\ T_{KR} &= \begin{bmatrix} 1 & 0 \\ \dfrac{1}{KR} & 1 \end{bmatrix} \\ T_{R/K} &= \begin{bmatrix} 1 & 0 \\ \dfrac{K}{R} & 1 \end{bmatrix}. \end{aligned} \tag{6}$$

Combining, (3) and (4), we get

$$\begin{aligned} I_{1i} &= I_{2i} + Y_{11} V_{2i} + Y_{12} V_{3i} \\ I_{4i} &= I_{3i} + Y_{21} V_{2i} + Y_{22} V_{3i}. \end{aligned} \tag{7}$$

Consequently, the four-port transmission matrix of the branch network in Fig. 4 may be written as

$$\begin{bmatrix} V_{1i} \\ V_{4i} \\ I_{1i} \\ I_{4i} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ Y_{11} & Y_{12} & 1 & 0 \\ Y_{21} & Y_{22} & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{2i} \\ V_{3i} \\ I_{2i} \\ I_{3i} \end{bmatrix} = [G]_{i,m} \begin{bmatrix} V_{2i} \\ V_{3i} \\ I_{2i} \\ I_{3i} \end{bmatrix}. \tag{8}$$

The transmission matrix of the four-port network in Fig. 2 may then be obtained

$$[TA]_m = \left(\prod_{i=1}^{N} [P]_{i,m} \times [G]_{i,m} \right) \times [P]_{N+1,m} \tag{9}$$

where $[G]_{i,m}$ and $[P]_{i,m}$ are obtained in (8) and (2), respectively, and $[P]_{N+1,m}$ is that of the last section. Consequently, the input voltages and currents in Fig. 2 are related to those at the output as

$$\begin{aligned} \begin{bmatrix} V_1 \\ V_4 \\ I_1 \\ I_4 \end{bmatrix} &= [TA] \begin{bmatrix} V_2 \\ V_3 \\ -I_2 \\ -I_3 \end{bmatrix} \\ &= \left[\begin{array}{cc:cc} T_{11} & T_{12} & T_{13} & T_{14} \\ T_{21} & T_{22} & T_{23} & T_{24} \\ \hdashline T_{31} & T_{32} & T_{33} & T_{34} \\ T_{41} & T_{42} & T_{43} & T_{44} \end{array}\right] \begin{bmatrix} V_2 \\ V_3 \\ -I_2 \\ -I_3 \end{bmatrix} \\ &= \begin{bmatrix} [C11] & [C12] \\ [C21] & [C22] \end{bmatrix} \begin{bmatrix} V_2 \\ V_3 \\ -I_2 \\ -I_3 \end{bmatrix} \end{aligned} \tag{10}$$

where we define the following sub-matrices:

$$\begin{aligned} [C11] &= \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \quad [C12] = \begin{bmatrix} T_{13} & T_{14} \\ T_{23} & T_{24} \end{bmatrix} \\ [C21] &= \begin{bmatrix} T_{31} & T_{32} \\ T_{41} & T_{42} \end{bmatrix} \quad [C22] = \begin{bmatrix} T_{33} & T_{34} \\ T_{43} & T_{44} \end{bmatrix}. \end{aligned} \tag{11}$$

On the other hand, the admittance matrix of a four-port network is

$$\begin{aligned} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} &= \left[\begin{array}{cc:cc} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ \hdashline Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{array}\right] \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \\ &= \begin{bmatrix} [Y11] & [Y12] \\ [Y21] & [Y22] \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \end{aligned} \tag{12}$$

where we may define the following sub-matrices:

$$[Y11]=\begin{bmatrix}Y_{11}&Y_{12}\\Y_{21}&Y_{22}\end{bmatrix}\quad[Y12]=\begin{bmatrix}Y_{13}&Y_{14}\\Y_{23}&Y_{24}\end{bmatrix}$$
$$[Y21]=\begin{bmatrix}Y_{31}&Y_{32}\\Y_{41}&Y_{42}\end{bmatrix}\quad[Y22]=\begin{bmatrix}Y_{33}&Y_{34}\\Y_{43}&Y_{44}\end{bmatrix}. \quad (13)$$

Therefore, the admittance matrix of the four-port network may be written as

$$\begin{bmatrix}[Y11]&[Y12]\\[Y21]&[Y22]\end{bmatrix}=\begin{bmatrix}[C22]\,[C12]^{-1}&[C21]-[C22]\,[C12]^{-1}\,[C11]\\-[C12]^{-1}&[C12]^{-1}\,[C11]\end{bmatrix}. \quad (14)$$

Now, since ports 1 and 4 in Fig. 2 are connected together, we have

$$V_1=V_4=V \quad (15)$$
$$I=I_1+I_4. \quad (16)$$

Applying (15) and (16) to (12), we obtain the admittance matrix of three-port network A in Fig. 1

$$\begin{bmatrix}I\\I_2\\I_3\end{bmatrix}=\begin{bmatrix}Y_{11}+Y_{14}+Y_{41}+Y_{44}&Y_{12}+Y_{42}&Y_{13}+Y_{43}\\Y_{21}+Y_{24}&Y_{23}&Y_{24}\\Y_{31}+Y_{34}&Y_{32}&Y_{33}\end{bmatrix}\times\begin{bmatrix}V\\V_2\\V_3\end{bmatrix}=[YA]\begin{bmatrix}V\\V_2\\V_3\end{bmatrix} \quad (17)$$

$$[YA]=\begin{bmatrix}y_{11}&y_{12}&y_{13}\\y_{21}&y_{22}&y_{23}\\y_{31}&y_{32}&y_{33}\end{bmatrix}. \quad (18)$$

Now we consider the $ABCD$ matrix of network B as

$$\begin{bmatrix}V_1\\I_1\end{bmatrix}=[TB]\begin{bmatrix}V\\I\end{bmatrix}\Rightarrow\begin{bmatrix}V\\I\end{bmatrix}=[TB]^{-1}\begin{bmatrix}V_1\\I_1\end{bmatrix}=\begin{bmatrix}\cosh\gamma_{FL,m}l_{FL}&Z_{FL,m}\sinh\gamma_{FL,m}l_{FL}\\Y_{FL,m}\sinh\gamma_{FL,m}l_{FL}&\cosh\gamma_{FL,m}l_{FL}\end{bmatrix}^{-1}\times\begin{bmatrix}V_1\\I_1\end{bmatrix}=\begin{bmatrix}t_{11}&t_{12}\\t_{21}&t_{22}\end{bmatrix}\begin{bmatrix}V_1\\I_1\end{bmatrix} \quad (19)$$

and obtain the admittance matrix of the three-port network by eliminating V and I among (17)–(19) and (20), shown at the bottom of this page.

Finally, we may drive its unnormalized scattering matrix

$$[S]=([YT]+[YL])^{-1}([YL]-[YT]) \quad (21)$$

where

$$[YL]=\begin{bmatrix}Y_{L1}&0&0\\0&Y_{L2}&0\\0&0&Y_{L3}\end{bmatrix}$$
$$Y_{L1}=\frac{1}{Z_{L1}}\quad Y_{L2}=\frac{1}{Z_{L2}}\quad Y_{L3}=\frac{1}{Z_{L3}}. \quad (22)$$

III. Construction of an Error Function

Since the source impedances (Z_{L1}, Z_{L2}, and Z_{L3}) have different values, we may normalize the scattering parameters by defining the normalized voltages as

$$\overline{V}_n^{\pm}=\frac{V_n^{\pm}}{\sqrt{Z_{Ln}}}. \quad (23)$$

Consequently, the normalized scattering matrix may be obtained from the unnormalized one as

$$\begin{bmatrix}\overline{V}_1^-\\\overline{V}_2^-\\\overline{V}_3^-\end{bmatrix}=\begin{bmatrix}S_{11}&\frac{\sqrt{Z_{L2}}}{\sqrt{Z_{L1}}}S_{12}&\frac{\sqrt{Z_{L3}}}{\sqrt{Z_{L1}}}S_{13}\\\frac{\sqrt{Z_{L1}}}{\sqrt{Z_{L2}}}S_{21}&S_{22}&\frac{\sqrt{Z_{L3}}}{\sqrt{Z_{L2}}}S_{23}\\\frac{\sqrt{Z_{L1}}}{\sqrt{Z_{L3}}}S_{31}&\frac{\sqrt{Z_{L2}}}{\sqrt{Z_{L3}}}S_{32}&S_{33}\end{bmatrix}\begin{bmatrix}\overline{V}_1^+\\\overline{V}_2^+\\\overline{V}_3^+\end{bmatrix}. \quad (24)$$

$$\Rightarrow\begin{bmatrix}I_1\\I_2\\I_3\end{bmatrix}=\frac{1}{(t_{22}-y_{11}t_{12})}\begin{bmatrix}(y_{11}t_{11}-t_{21})&y_{12}&y_{13}\\y_{21}&y_{22}(t_{22}-y_{11}t_{12})+y_{21}t_{12}y_{12}&y_{23}(t_{22}-y_{11}t_{12})+y_{21}t_{12}y_{13}\\y_{31}&y_{32}(t_{22}-y_{11}t_{12})+y_{31}t_{12}y_{12}&y_{33}(t_{22}-y_{11}t_{12})+y_{31}t_{12}y_{13}\end{bmatrix}\begin{bmatrix}V_1\\V_2\\V_3\end{bmatrix}=[YT]\begin{bmatrix}V_1\\V_2\\V_3\end{bmatrix} \quad (20)$$

Thus, we may assume that all three ports have impedances equal to unity.

We then construct an error function as

$$\varepsilon = W1\sum_{m=1}^{M}\left|\overline{S}_{23,m}\right|^2 + W2\sum_{m=1}^{M}\left[\left|\overline{S}_{21,m}\right|^2 - \frac{1}{1+K^2}\right]^2 + W3\sum_{m=1}^{M}\left[\left|\overline{S}_{31,m}\right|^2 - \frac{K^2}{1+K^2}\right]^2 \quad (25)$$

where $\overline{S}_{23,m} = (\sqrt{Z_{L3}}/\sqrt{Z_{L2}})S_{23,m}$ and $\overline{S}_{21,m} = (\sqrt{Z_{L1}}/\sqrt{Z_{L2}})S_{21,m}$ and also $S_{21,m}$ and $S_{23,m}$ are obtained from (21). $W1$, $W2$, and $W3$ are weighting functions, which may adjust the values of the three terms by the design specifications. They could, in general, be functions of frequency. The required bandwidth is divided into M discrete frequencies, which are denoted by the subscript m. $\overline{S}_{23,m}$ is now the isolation between the two outputs, which should ideally be equal to zero. As it was assumed earlier that the output power from port 3 be equal to K^2 times that from port 2, we then specify that $\left|\overline{S}_{21,m}\right|^2 = 1/(1+K^2)$ and $\left|\overline{S}_{31,m}\right|^2 = K^2/(1+K^2)$. The error is a function of widths and lengths of various line sections.

The minimization of the error function with respect to the parameters of the geometrical configuration (namely, lengths and widths of transmission lines) of the power divider may be performed by the genetic algorithm or the conjugate gradient method or a combination of the two. However, for some algorithms, we may need to specify the initial values for the variables. We may select them by a random generator, but here we present a method for the computation of initial values of the divider variables, which may actually be considered as a first attempt at its design. This procedure ensures us to finally obtain a realizable power divider.

The commercial simulation softwares, such as HFSS, do not provide any initial design of the microwave components and are at best a blind process and very CPU time consuming. Furthermore, as the dimensions of the components (such as the lengths and widths of line sections) vary, the circuit parts may get disconnected. Consequently, the design and optimization of microwave components by such software are actually complex and tedious processes.

IV. Determination of the Initial Values of Divider Parameters

For the evaluation of approximate initial values of the parameters at the center frequency, we use the even- and odd-mode analysis, even though the divider is not strictly symmetrical. We assume that the upper and lower half-circuits are electrically identical and the values of their characteristic impedances are proportional. Since it is assumed that the power flow in the lower half circuit is equal to K^2 times that in the upper half circuit, it is required that the characteristic impedances of the upper half circuit be K^2 times those in the lower one. Since in the general case $Z_{L2} \neq K^2 Z_{L3}$, then in Fig. 1 we consider the line sections $Z_{SU(N+1)}$ and $Z_{SD(N+1)}$ as impedance transformers at the center frequency for Z_{L2} to KZ_0 and Z_{L3} to Z_0/K,

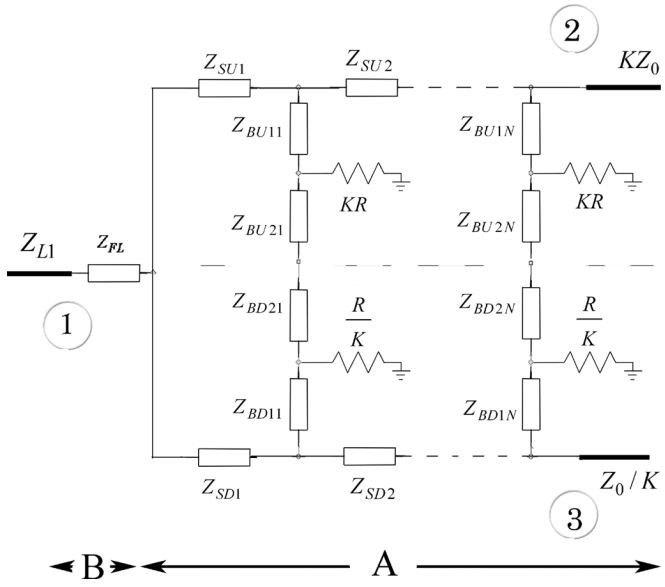


Fig. 5. Transformation of circuit in Fig. 1 for the purpose of calculation of initial values of circuit elements.

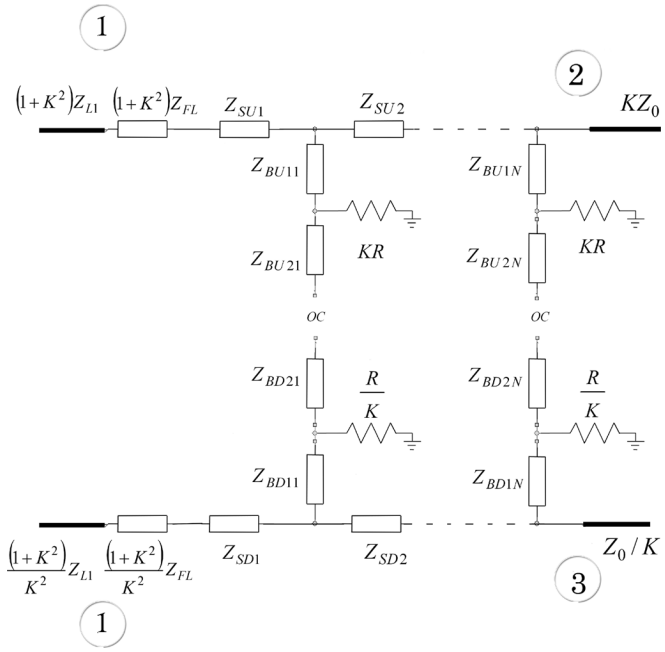


Fig. 6. Equivalent circuit in Fig. 5 in the case of even-mode excitation.

respectively. Therefore, the characteristic impedance of lines $Z_{SU(N+1)}$ and $Z_{SD(N+1)}$ (assuming that their initial lengths are equal to a quarter-wavelength at the center frequency) are obtained. The circuit in Fig. 5 may then be arrived at. The inclusion of single line sections Z_{FL}, $Z_{SU(N+1)}$, and $Z_{SD(N+1)}$ at the output ports are intended for some rough narrowband impedance matching at the center frequency and also connection paths to the terminals. However, the whole circuit configuration of the power divider provides the specified power division ratios and impedance matching among the output ports, which are realized by the proposed design and optimization procedure. The wideband impedance-matching function of the circuit is not achieved by the line sections Z_{FL}, $Z_{SU(N+1)}$, and $Z_{SD(N+1)}$

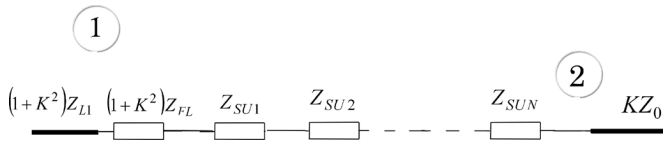


Fig. 7. Equivalent circuit between ports 1 and 2 in Fig. 6 at the center frequency with all the transmission line circuit lengths equal to a quarter-wavelength.

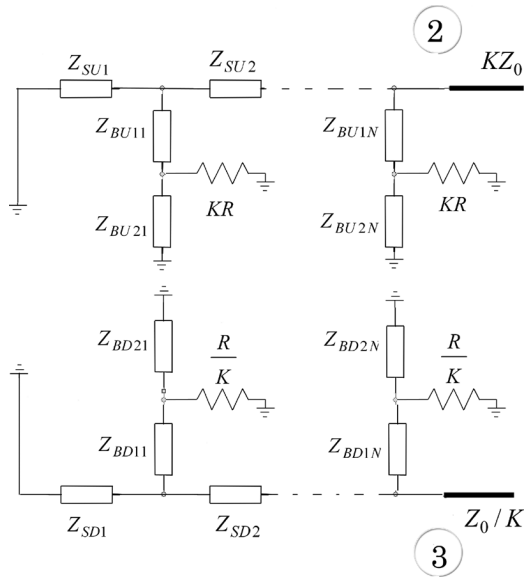


Fig. 8. Equivalent circuit of network in Fig. 5 for the odd-mode excitation of ports 2 and 3.

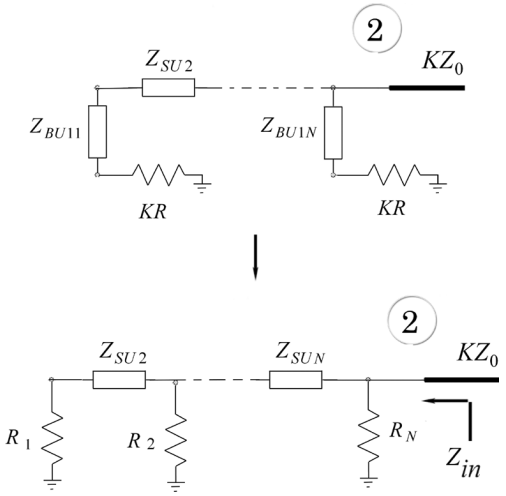


Fig. 9. Circuit transformations of networks connected to port 2 in Fig. 8 at the center frequency.

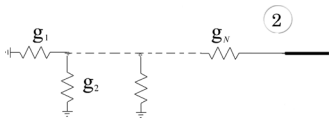
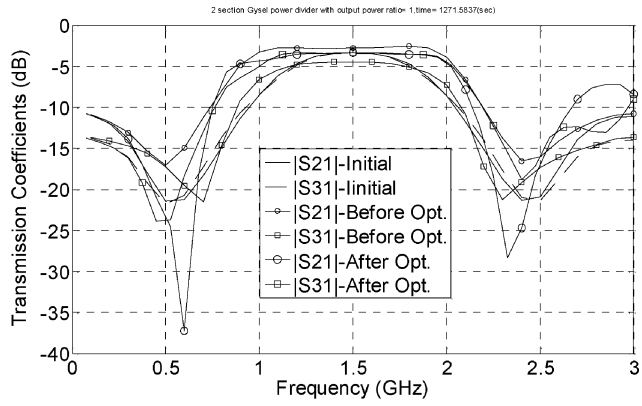


Fig. 10. Resistive ladder network.

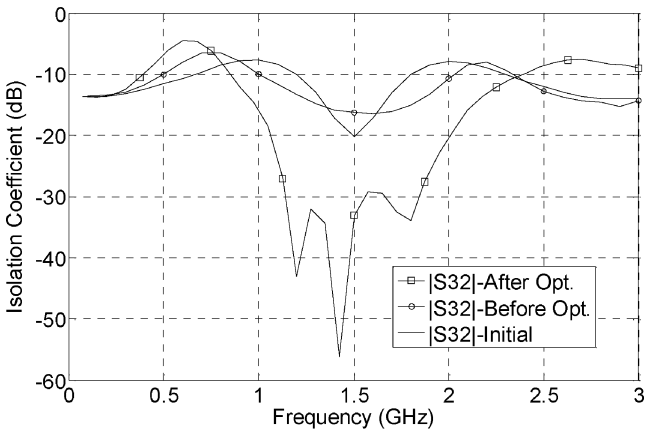
(which is, at best, narrowband and may actually increase the circuit size), but rather it is inherently realized by the whole circuit configuration. The lengths of these line sections may be minimized through the design procedure.

TABLE I
COMPUTER PROGRAM PARAMETERS AND THEIR DEFINITIONS

Parameter	Definition
N	number of sections of power divider
ε_r	dielectric constant of substrate
h	Substrate thickness
Loss tan.	loss tangent of substrate at frequency 10 GHz
Dispersion selection	selects the dielectric dispersion model; if 0 $\Rightarrow$ no dispersion model is used ; if 1 $\Rightarrow$ Kirschning and Jansen dispersion model is used which is valid upto 60 GHz [11]
Sigma	Metal conductivity of microstrip lines
f_L	lower limit of frequency bandwidth
f_U	upper limit of frequency bandwidth
M	number of discrete frequencies in the bandwidth
K^2	Power division ratio (P_3/P_2)
Z_{Li}	Impedance of i'th port
Min. W	the minimum allowable widths of all the strips in the main and branch lines. This limit is required for the strips to be easily fabricated by available technology



(a)



(b)

Fig. 11. Frequency responses of example 1 as obtained by the proposed design algorithm. (a) Transmission coefficients. (b) Isolation coefficient.

If this circuit is excited by an even mode at the outputs 2 and 3 by voltages with equal amplitudes, the circuit in Fig. 6

TABLE II
DATA FOR EXAMPLE 1 AS OBTAINED BY THE PROPOSED DESIGN ALGORITHM

Input Values											
N=2, $P_3/P_2 = K^2 = 1$, ε_r =10.2 , h=1.27 mm , *loss tan.*=0.002 , f_L=1 GHz , M=30, f_U =2 GHz, *Sigma*= 5.7e7 S/m *Dispersion Selection*=1, Z_{L1} =50 Ohm , Z_{L2} =50 Ohm, Z_{L3} =100 Ohm , *Min.W*=0.01 mm, *Error-Init.*=4.3133, *Error-After opt.*=0.28201											
Initial Variable Values **(mm)**				***Variable Values Before Final Optimization*** **(mm)**				***Variable Values After Final Optimization*** **(mm)**			
W_{FL}	1.62	L_{FL}	18.75	W_{FL}	1.18	L_{FL}	18.75	W_{FL}	0.86	L_{FL}	11.55
W_{SU1}	0.29	L_{SU1}	19.81	W_{SU1}	1.54	L_{SU1}	19.81	W_{SU1}	0.76	L_{SU1}	19.92
W_{SU2}	0.29	L_{SU2}	19.81	W_{SU2}	1.64	L_{SU2}	19.81	W_{SU2}	1.93	L_{SU2}	39.38
W_{SU3}	0.81	L_{SU3}	19.3	W_{SU3}	1.41	L_{SU3}	19.3	W_{SU3}	2.8	L_{SU3}	9.42
W_{BU11}	0.84	L_{BU11}	19.27	W_{BU11}	1.56	L_{BU11}	19.27	W_{BU11}	1.89	L_{BU11}	21.02
W_{BU12}	0.56	L_{BU12}	19.5	W_{BU12}	0.47	L_{BU12}	19.5	W_{BU12}	0.3	L_{BU12}	10.46
W_{BU21}	4.14	L_{BU21}	17.82	W_{BU21}	3.81	L_{BU21}	17.82	W_{BU21}	6.35	L_{BU21}	16.88
W_{BU22}	4.14	L_{BU22}	17.82	W_{BU22}	3.81	L_{BU22}	17.82	W_{BU22}	4.92	L_{BU22}	30.79
W_{SD1}	0.29	L_{SD1}	19.81	W_{SD1}	0.66	L_{SD1}	19.81	W_{SD1}	0.86	L_{SD1}	20.12
W_{SD2}	0.29	L_{SD2}	19.81	W_{SD2}	1.73	L_{SD2}	19.81	W_{SD2}	2.48	L_{SD2}	39.13
W_{SD3}	0.3	L_{SD3}	19.79	W_{SD3}	0.83	L_{SD3}	19.79	W_{SD3}	1.25	L_{SD3}	15.8
W_{BD11}	0.84	L_{BD11}	19.27	W_{BD11}	1.73	L_{BD11}	19.27	W_{BD11}	1.4	L_{BD11}	20.76
W_{BD12}	0.56	L_{BD12}	19.5	W_{BD12}	0.47	L_{BD12}	19.5	W_{BD12}	0.87	L_{BD12}	14.14
W_{BD21}	4.14	L_{BD21}	17.82	W_{BD21}	3.53	L_{BD21}	17.82	W_{BD21}	4.73	L_{BD21}	14.11
W_{BD22}	4.14	L_{BD22}	17.82	W_{BD22}	3.76	L_{BD22}	17.82	W_{BD22}	6.35	L_{BD22}	13.69

may be obtained because the upper and lower half circuits are electrically symmetric.

For the realization of electrical symmetry of the network, the initial variable values should have the following relations:

$$\begin{aligned} Z_{SUi} &= K^2\ Z_{SDi} \\ Z_{BU1i} &= K^2\ Z_{BD1i} \\ Z_{BU2i} &= K^2\ Z_{BD2i} \\ \beta_{SUi,f_0}\, l_{SUi} &= \beta_{SDi,f_0}\, l_{SDi} \\ \beta_{BU1i,f_0}\, l_{BU1i} &= \beta_{BD1i,f_0}\, l_{BD1i}, \\ &\quad \text{where } f_0 \text{ is the center frequency} \\ \beta_{BU2i,f_0}\, l_{BU2i} &= \beta_{BD2i,f_0}\, l_{BD2i}. \end{aligned} \tag{26}$$

The transmission line sections Z_{FL} and Z_{L1} in Fig. 5 are considered as parallel combination of two transmission lines placed in the upper and lower half circuits, as in Fig. 6, with characteristic impedances in the ratio of K^2 having the same electrical lengths at the center frequency.

Now, since the reflection coefficients at ports 2 and 3 should be equal to zero, then the network between ports 1 and 2 should match the impedance KZ_0 to impedance $\left(1+K^2\right)Z_{L1}$. If the initial lengths of all the line sections are equal to a quarter-wavelength at the center frequency, then the impedance seen at the junction of the main line and the branch lines would be infinity and are actually open circuited, as is seen from the equivalent circuit for the even-mode excitation in Fig. 6.Its equivalent circuit may then be represented as in Fig. 7.

There are different methods for the computation of characteristic impedances of the line sections (Z_{SUi}) in Fig. 7. However, for simplicity, we choose the arithmetic (or geometric) mean of KZ_0 and $\left(1+K^2\right)Z_{L1}$ for all of them.

For the evaluation of proper initial values for the characteristic impedances of all the other line sections, we refer to the equivalent circuit of the odd-mode excitation in Fig. 5. Now, since the excitation voltage at port 2 is equal to K^2 times that at port 3, the impedances of the upper half circuit are also equal to K^2 times those of the lower one, and then the current distributions in the upper and lower half circuits are equal. Consequently, the odd-mode equivalent circuit may be drawn as in Fig. 8.

Since the lengths of all the line sections are equal to a quarter-wavelength, the half circuit connected to port 2 is reduced to a resistive circuit, as shown in Fig. 9, where the line sections Z_{BU2i} may be removed.

The input impedance of the network in Fig. 9 may be written in the form of continued fractions, which should be equal to KZ_0, so that impedance matching is achieved at the center frequency. The input impedance of the network in Fig. 9 is similar to that in Fig. 10. There are available design tables in [10] for the evaluation of parameters g_i to achieve impedance matching. With due consideration of the similarity between the networks in Figs. 9 and 10, the values of R_i in Fig. 9 may be determined.

The initial values of Z_{BU2i} are arbitrarily set equal to $25\times K^2\ \Omega$. The value of resistor R is set equal to $47\ \Omega$. The initial values of characteristic impedances Z_{BU1i} of line sections may be obtained from the known values of KR and R_i.

Since the divider circuit in Fig. 5 has electrical symmetry along its center line, the characteristic impedance of the line sections in the lower half are equal to $1/K^2$ times those in the

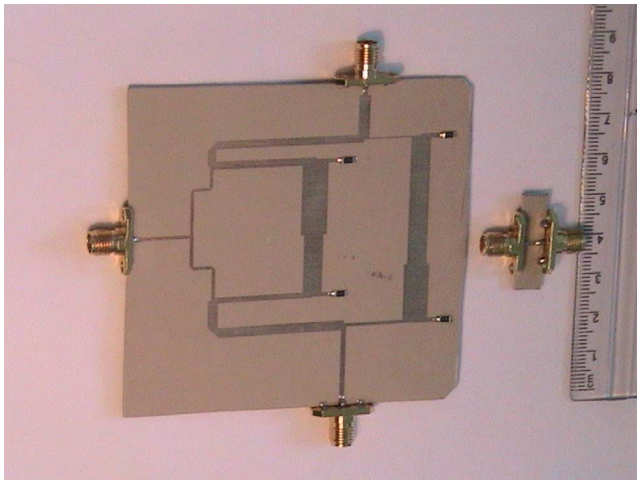


Fig. 12. (*left*) Photograph of fabricated two-section power divider of example 1 (*right*) component used to measure additional phase difference caused by connectors and 50-Ω transmission lines connected to ports.

upper half. The lengths of line sections are all equal to a quarter-wavelength at the center frequency.

V. Examples of Numerical Design, Fabrication, and Measurements

In this section, we present two examples of numerical design, computer simulation, fabrication, and measurement of a multisection power divider. We use the substrate RT-Duroid 6010 with dielectric constant $\varepsilon_r = 10.2$, thickness $h = 1.27$ mm, and loss tangent $\tan\sigma = 0.002$. The dielectric and conductor losses and dispersion effects are considered by using the closed-form formulas available in the literature. The characteristic impedances of line sections may be obtained by the formulas available in the literature [11]–[13].

Two examples with different power division ratios, different load impedances, and different frequency intervals are considered. The results of the proposed numerical design procedure are evaluated by simulation software HFSS version 11 and also fabrication and measurement.

The algorithm for the proposed design and optimization procedure is coded by MATLAB software [14]. The input design parameters for the numerical computer programs are defined in Table I and are provided by the design engineer. The initial values of the dimensions of the power divider are given in tables under the heading of "Initial Variable Values (mm)" and their corresponding frequency response curves are drawn in figures denoted by "initial." The value of error function for those initial values is given at the top of tables denoted by "Error-Init." The lengths of line sections are then kept constant and the optimization is carried out on the widths of line sections by the proposed design procedure. The values obtained for the linewidths at this stage are given in tables under the heading of "Variable Values before Final Optimization (mm)." The scattering parameters are calculated and drawn in the figures versus frequency, where they are denoted by "Before Opt."

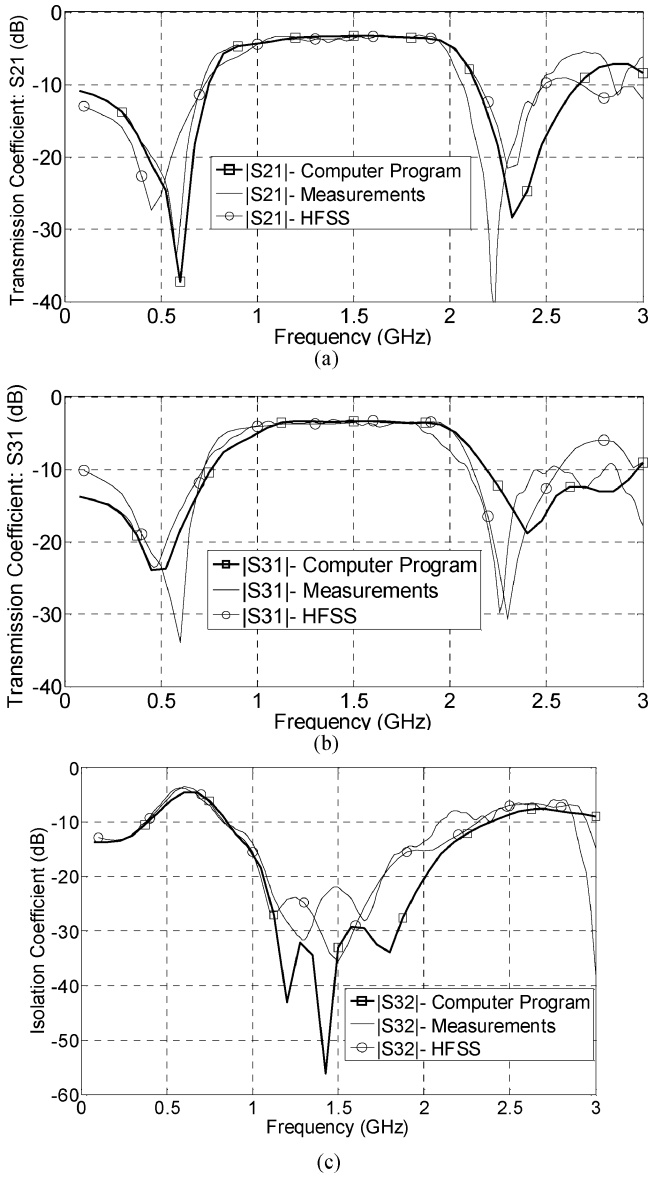


Fig. 13. Comparison of frequency responses obtained by the proposed design algorithm, simulation software, and measurement data for example 1. (a) $S21$ coefficient. (b) $S31$ coefficient. (c) $S32$ coefficient.

Finally, the optimization is carried out simultaneously on all the dimensions of the divider, namely, line lengths and widths. The frequency response curves of scattering parameters for the optimum divider are drawn in the figures and denoted by "After Opt." The value of error is denoted by "Error-After opt." and written at the top of tables.

The computer programs are run on the personal computer Core 2 Duo CPU @2.4 GHz and the CPU time in seconds is written at the top of figures.

1) Example I: In the first example, we consider a two-section power divider with equal power division between the two output ports 2 and 3. The impedances at ports 1 and 2 are equal to 50 Ω and that at the output port 3 is equal to 100 Ω. If we were to use the even- and odd-mode analysis for this example (with equal power division between output ports), then it would have been necessary to keep the impedances at the output ports identical. However in example 1, the input and

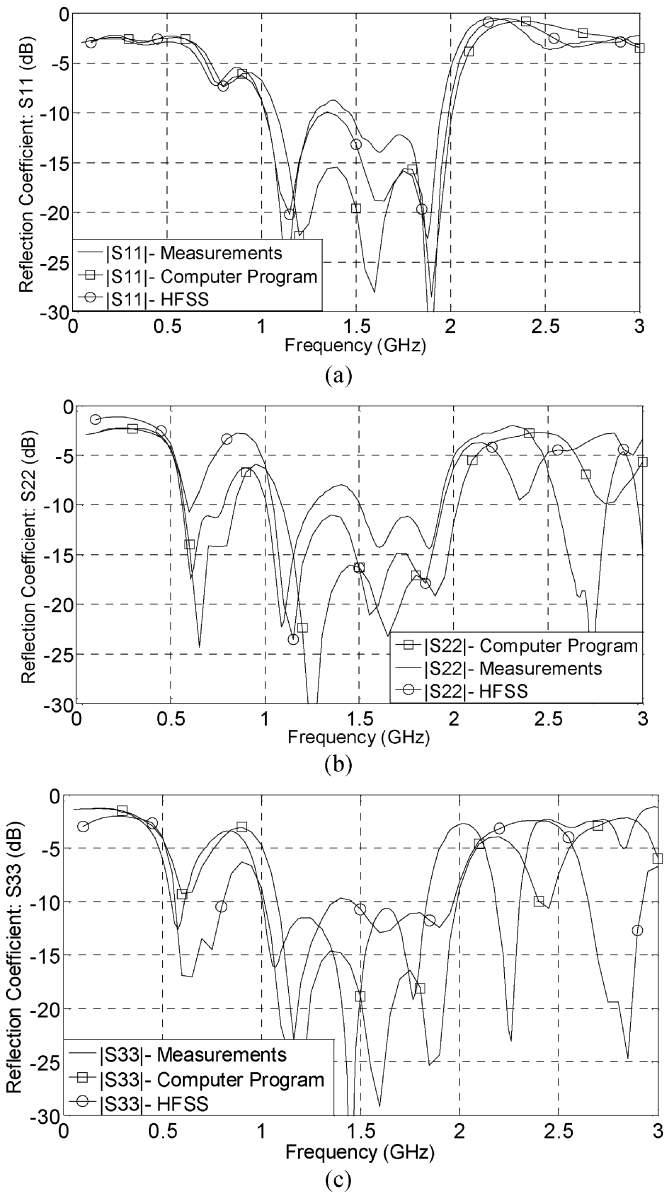


Fig. 14. Comparison between frequency responses of the first design example determined by the method of least squares computer program, HFSS software and measurements. (a) Reflection coefficient S_{11}, (b) S_{22}, and (c) S_{33}.

output impedances are selected unequal, in order to highlight the capability of the proposed design method. The L frequency band (1–2 GHz) is adopted. All the internal resistors of the circuit are considered constant equal to the standard value of 47 Ω and are selected as common surface mount device (SMD) chip resistors. The results of the optimum design by the method of least squares are drawn in Fig. 11 and given in Table II. The -5-dB bandwidth of the transmission coefficient S_{21} has also increased by 200 MHz.

The optimum design of the divider is simulated by the HFSS software. It is also fabricated and its photograph is shown in Fig. 12. Note that the optimum values of geometrical parameters of the divider configuration are obtained by the proposed design algorithm (coded in MATLAB), and not by HFSS software. The data obtained by the full-wave analysis through HFSS is merely for the purpose of comparison and

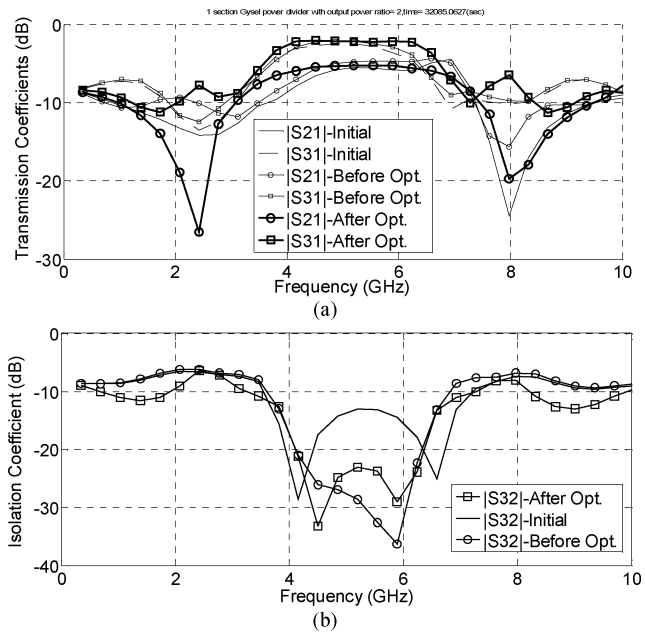


Fig. 15. Frequency responses of example 2 as obtained by the proposed design algorithm.

validation of our design method. Its frequency response is measured by the network analyzer HP8722ES. The performances of the proposed optimum design algorithm, HFSS software simulation, and measurement data are compared in the Fig. 13 with excellent agreement.

In this example, the measured values of scattering parameters on the basis of 50-Ω impedance are converted to those for the actual input/output impedances by the relations that are explained in detail in [15] and [16].

We assume that all the ports of the power divider have identical impedances equal to 50 Ω and measure its scattering parameters by the usual methods and measurement equipment. We may then use the generalized scattering matrix to calculate the scattering parameters of the power divider for different source and load impedances equal to $Z_{L1} = 50\ \Omega$, $Z_{L2} = 50\ \Omega$, and $Z_{L3} = 100\ \Omega$.

We have fabricated a component (shown on the right side of Fig. 12) composed of two SMD connectors and a 50-Ω line section between them, of which the length is equal to the sum of extra 50-Ω line sections included at the divider terminals. The phase difference of this component is measured and subtracted from the measured phase differences of the divider. Thus, the exact phase differences among the divider terminals may be determined.

In Fig. 14, the results of the proposed design algorithm, full-wave simulation software, and measurement data of the reflection coefficients at the input and output ports of divider (namely, S_{11}, S_{22}, and S_{33}) are drawn for comparison. Although, these reflection coefficients are not explicitly included in the error function, they exhibit a good frequency response in the specified bandwidth, which attest to the correct implementation of impedance matching.

2) Example II: In the second example, we consider a single-section power divider with unequal power division at its output ports and identical impedances at its terminals (equal to

TABLE III
DESIGN DATA OF EXAMPLE 2 AS OBTAINED BY THE PROPOSED COMPUTER ALGORITHM

Input Values											
N=1, $P_3 / P_2 = K^2 = 2$, ε_r =10.2, h=1.27 mm, *loss tan.*=0.002, f_L=3.8 GHz, M=30, f_U =6.6 GHz, *Sigma*= 5.7e7 S/m *Dispersion Selection*=1, Z_{L1} =50 Ohm, Z_{L2} =50 Ohm, Z_{L3} =50 Ohm, *Min.W*=0.01 mm, *Error-Init.*=2.3829, *Error-After opt.*=0.54522											
Initial Variable Values (mm)				***Variable Values Before Final Optimization*** (mm)				***Variable Values After Final Optimization*** (mm)			
W_{FL}	2.11	L_{FL}	5.2	W_{FL}	1.48	L_{FL}	5.2	W_{FL}	1.5	L_{FL}	4.42
W_{SU1}	0.11	L_{SU1}	17.24	W_{SU1}	0.24	L_{SU1}	17.24	W_{SU1}	0.13	L_{SU1}	17.24
W_{SU2}	0.81	L_{SU2}	16.38	W_{SU2}	0.68	L_{SU2}	16.38	W_{SU2}	0.27	L_{SU2}	10.9
W_{BU11}	0.88	L_{BU11}	5.44	W_{BU11}	0.66	L_{BU11}	5.44	W_{BU11}	1.24	L_{BU11}	5.69
W_{BU21}	1.19	L_{BU21}	5.37	W_{BU21}	1.02	L_{BU21}	5.37	W_{BU21}	3.44	L_{BU21}	6.03
W_{SD1}	0.96	L_{SD1}	16.27	W_{SD1}	1.06	L_{SD1}	16.27	W_{SD1}	0.78	L_{SD1}	16.94
W_{SD2}	1.67	L_{SD2}	15.81	W_{SD2}	1.89	L_{SD2}	15.81	W_{SD2}	0.41	L_{SD2}	11.18
W_{BD11}	3.43	L_{BD11}	5.05	W_{BD11}	2.79	L_{BD11}	5.05	W_{BD11}	1.23	L_{BD11}	5.3
W_{BD21}	4.14	L_{BD21}	4.99	W_{BD21}	3.81	L_{BD21}	4.99	W_{BD21}	4.04	L_{BD21}	3.81

50 Ω). The output power at port 3 is twice that at port 2. If we were to use the even- and odd-mode analysis for this example (with unequal power division at the outputs), it would have been necessary to have the impedances at the two output ports unequal (namely, the impedance of port 2 equal to 100 Ω). However in example 2, the input and output impedances are selected equal in order to highlight the capability of the proposed design method.

The frequency bandwidth is selected in the range of 3.8–6.6 GHz. The internal resistors in the upper half of the circuit are selected equal to 66 Ω, which are made as the series connection of two standard chip resistors of 33 Ω. The internal resistors in the lower half of the circuit are selected as the standard 33-Ω chip resistors.

In this example, we have also included the phase difference between ports 2 and 3 in the error function in (27) where the weighting functions are selected as $W1 = W2 = W3 = 1$ and $W4 = 0.25$. We have selected the initial line lengths in the upper and lower series line equal to $3\lambda/4$ of the center frequency because, in the selected frequency bandwidth and for the selected substrate thickness, the length of the quarter-wavelength is too short

$$\varepsilon = W1 \sum_{m=1}^{M} \left|\overline{S}_{23,m}\right|^2 + W2 \sum_{m=1}^{M} \left[\left|\overline{S}_{21,m}\right|^2 - \frac{1}{1+K^2}\right]^2 + W3 \sum_{m=1}^{M} \left[\left|\overline{S}_{31,m}\right|^2 - \frac{K^2}{1+K^2}\right]^2 + W4 \sum_{m=1}^{M} \left[\angle\left(\overline{S}_{21,m}\right) - \angle\left(\overline{S}_{31,m}\right)\right]^2. \quad (27)$$

The frequency responses obtained from the proposed design algorithm are drawn in Fig. 15 and the design data are given in Table III.

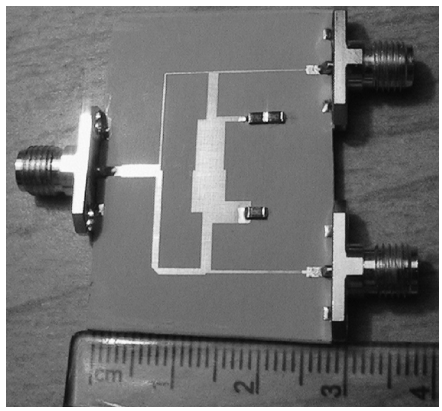


Fig. 16. Photograph of the single section power divider of example 2 as obtained by the design data in Table III.

The photograph of the divider is given in Fig. 16. The frequency responses of the designed power divider are obtained by the proposed algorithm, HFSS simulation software, and measurement data, and are drawn in Fig. 17 for comparison. In Fig. 18, the results of proposed design algorithm, full-wave simulation software, and measurement data of the reflection coefficients at the input and output ports of divider (namely, S_{11}, S_{22}, and S_{33}) are drawn for comparison.

The discrepancy among these data may be due to the parasitic effects of T-junctions (which are not taken into account in the computer program models and are more intense at higher frequencies), parasitic effects of common chip resistors at higher frequencies, connector losses and mismatches, and fabrication and measurement errors. As it is expected, the performance of the two-section power divider is superior to that of the single-section divider.

The phase response of the divider, as obtained by the HFSS software, is drawn in Fig. 19. The values of input parameters of the computer program, as given in Table I, are completely

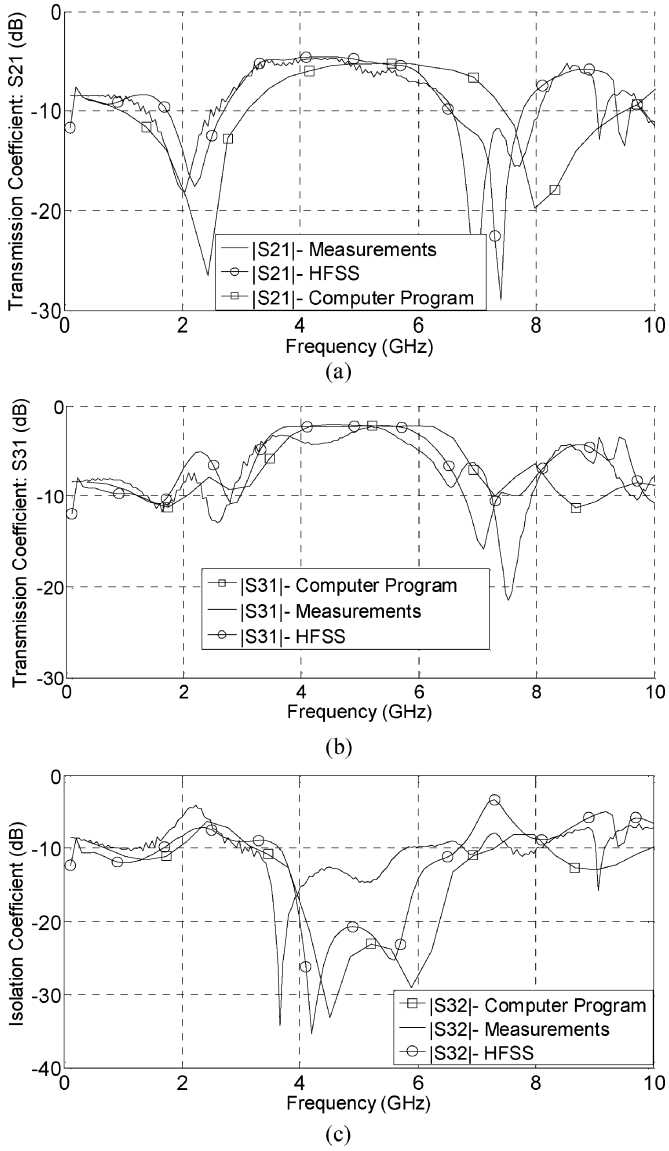


Fig. 17. Comparison of frequency responses of the single section power divider of example 2 as obtained by the proposed design algorithm, HFSS software and measurement data. (a) $S21$ coefficient. (b) $S31$ coefficient. (c) $S32$ coefficient.

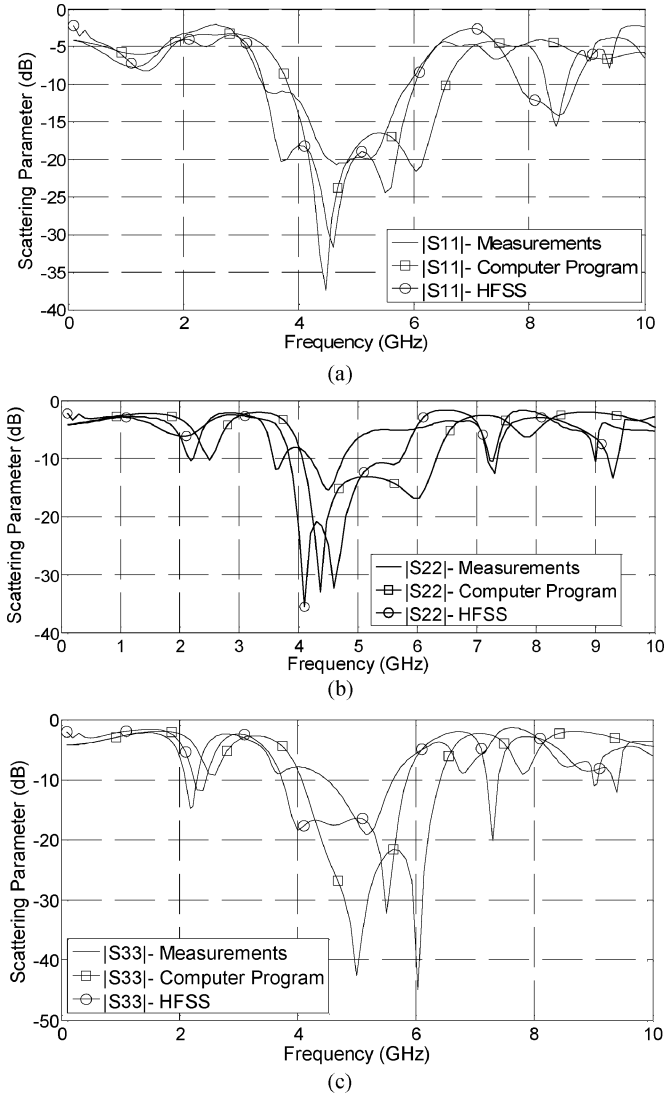


Fig. 18. Comparison between frequency responses of the second design example determined by the method of least squares computer program, HFSS software and measurements. (a) Reflection coefficient S_{11}, (b) S_{22}, and (c) S_{33}.

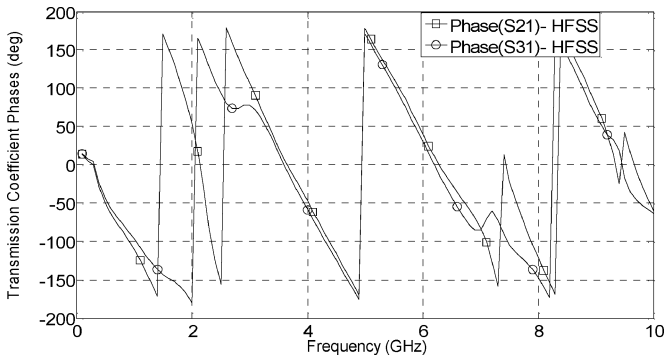


Fig. 19. Phase response of the divider for example 2 as obtained by the HFSS simulation software.

general. The optimum design of the divider gives the geometrical dimensions of the divider, which optimally realizes the design specifications. However, due to photolithography fabrication technology of microstrip circuits, the widths and lengths of line sections should be specified between some constraints, which are due to special limitations of realization of high- and low-impedance values. For example, the minimum values of the widths of lines are specified as *Min. W* in Table I. The maximum values of widths, which may cause overlapping of parallel lines, is not a limitation here.

3) Example III: Consider the design of a double-section power divider with the power division ratio 1:5, terminal port impedances $Z_{L1} = 50\,\Omega$, $Z_{L2} = 60\,\Omega$, and $Z_{L3} = 70\,\Omega$. The frequency interval is 5–8 GHz. The upper and lower branch resistances are $KR = 125\,\Omega$ and $R/K = 25\,\Omega$, respectively.

The selected substrate is RT-Duroid 6010. The output parameters of the design computer program are given in Table IV. The performance of the designed divider as the frequency responses of its scattering parameters is drawn in Fig. 20. Note that the optimum design procedure is performed here in one step from

TABLE IV
DATA FOR EXAMPLE 3 AS OBTAINED BY THE PROPOSED DESIGN ALGORITHM

Input Values			
N=2, $P_3/P_2 = K^2 = 5$, ε_r =10.2, h=1.27 mm, *loss tan.*=0.002, f_L=5 GHz, M=30, f_U =8 GHz, *Sigma*= 5.7e7 S/m			
Dispersion Selection=1, Z_{L1} =50 Ohm, Z_{L2} =60 Ohm, Z_{L3} =70 Ohm, *Min.W*=0.01 mm, *Error-Init.*=11.686, *Error-After opt.*=0.29732			
Initial Variable Values **(mm)**			
W_{FL}	2.08	L_{FL}	4.12
W_{SU1}	0.0013	L_{SU1}	14.14
W_{SU2}	0.0013	L_{SU2}	14.14
W_{SU3}	0.21	L_{SU3}	13.55
W_{BU11}	0.085	L_{BU11}	4.59
W_{BU12}	0.12	L_{BU12}	4.59
W_{BU21}	0.06	L_{BU21}	4.61
W_{BU22}	0.06	L_{BU22}	4.61
W_{SD1}	1.5	L_{SD1}	12.61
W_{SD2}	1.5	L_{SD2}	12.61
W_{SD3}	1.47	L_{SD3}	12.63
W_{BD11}	4.56	L_{BD11}	3.93
W_{BD12}	5.08	L_{BD12}	3.9
W_{BD21}	4.14	L_{BD21}	3.95
W_{BD22}	4.14	L_{BD22}	3.95
Variable Values After Final Optimization **(mm)**			
W_{FL}	1.88	L_{FL}	4.34
W_{SU1}	0.13	L_{SU1}	14.14
W_{SU2}	1.61	L_{SU2}	14.14
W_{SU3}	1.69	L_{SU3}	18.8
W_{BU11}	2.71	L_{BU11}	4.94
W_{BU12}	0.13	L_{BU12}	3.66
W_{BU21}	6.35	L_{BU21}	5.44
W_{BU22}	2.02	L_{BU22}	6.88
W_{SD1}	1.97	L_{SD1}	13.25
W_{SD2}	1.68	L_{SD2}	13.88
W_{SD3}	1.05	L_{SD3}	19.74
W_{BD11}	0.84	L_{BD11}	4.16
W_{BD12}	0.13	L_{BD12}	3.81
W_{BD21}	4.77	L_{BD21}	1.67
W_{BD22}	6.35	L_{BD22}	3.31

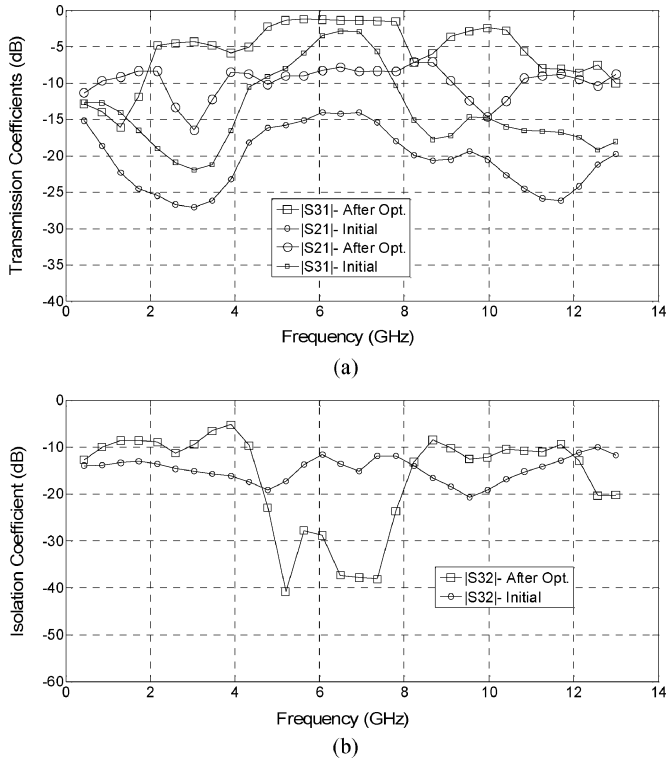


Fig. 20. Frequency responses of example 3 as obtained by the proposed design algorithm. (a) Transmission coefficients. (b) Isolation coefficient.

the initial case to the final design (designated as After Opt.). The design of this example was not fabricated.

VI. CONCLUSIONS

In this paper, a general method has been developed for the analysis of an asymmetrical multisection high power divider, which may account for arbitrary power division ratios at its output and arbitrary impedance matching at its input and output ports. Such a general power divider may not be analyzed by the conventional even- and odd-mode method, which is applicable to symmetrical devices. The scattering parameters of the divider are first derived by the proposed method. An optimum design procedure is then developed by the application of the method of least squares in order to construct an error function. Its minimization leads to the determination of the dimensions of the microstrip line sections. An approximate design procedure is also introduced based on the even- and odd-mode analysis, which may serve as an initial design for the optimization algorithm. Two examples of single- and two-section power dividers are designed, where specifications are made for unequal power division ratios and arbitrary impedances at the input and output ports. The performances of the designed power dividers as the frequency responses of isolation and transmission coefficients were obtained by the proposed algorithm, HFSS simulation software, fabrication, and measurement data. These results verify the efficacy of the proposed method of analysis of the power divider and the proposed optimum design procedure based on the method of least squares A two-section power divider with unequal port impedances is designed by the proposed method, which achieves a measured isolation of better than -22 dB in 44% of the L-band. The proposed analysis method and optimum design procedure may potentially be applicable to other microwave devices.

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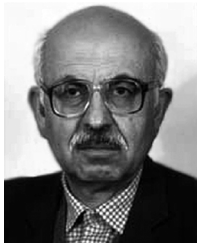

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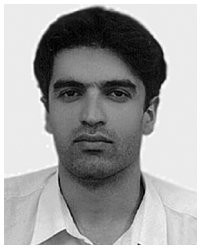

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